Project Title : **SiGe for MOS technologies Phase 2: development and applications**

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Start Date : 1st March 2001
End Date : 28th February, 2004

Investigators : Professor John Barker, Prof. A. Asenov, Dr. S. Roy,
Total Award : £ 4.1 million
Award to Glasgow : £ 411519

Academic Collaborators : Consortium on SiGe for MOS technology

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Project Summary :

An applications-driven, multi-disciplinary co-ordinated research activity involving fourteen research teams from nine universities and four industry partners. The project concerns the demonstration at device, circuit and system level, industrially significant performance enhancements (analogue and digital) available in Si MOS technologies through the incorporation of Si-Ge. The proposal consolidates and extends current activity by the existing consortium (Phase I group) and incorporates improved process schedules and a new management structure with strong links between device teams and circuit designers. Further performance improvements in both pseudomorphic and virtual substrate based devices will be sought down to 100 nm gatre lengths and performance evaluations in RF, micropower and digital CMOS circuitry will be made. The flagship demonstrator is a full RF receiver implemented in SiGe. New approaches to virtual substrate, active layer growth and process integration are included. The programme brings together teams working on device design and simulation (Glasgow) epitaxial layer growth, process development, electrical and structural characxterisation and circuit/system designers with an overall aim to establish a UK infrastructure which is the world focus for SiGe MOS work, with commercial potential and the capability of attracting world-wide interest and investment.

Project Objectives :

Development of next generation SiGe simulation tools and methodologies including:

a) Coupled n- and p- channel 2D full band Monte Carlo, finite element simulator for complete CMOS simulation with extensive RF analysis capability.
b) Full band 3D Monte Carlo simulator, incorporating first order quantum effects, ab initio interface roughness and Coulomb scattering and allowing predictive simulation of decanano SiGe devices.
c) Thorough calibration of the above simulators and new models against available experimental results from consortium partners both n industry and academe.
d) Extension of our methodology for parameterisation/calibration of commercial TCAD tools to allow the new generation of object oriented TCAD a SiGe device capability.

Employ our hierarchy of simulation tools in order to:

a) Design SiGe layer structures and device architectures according to the requirements of the consortium partners including highly linear RF nMOS devices with gate lengths to 100 nm, high drive current analogue and digital pMOS and nMOS devices with gate lengths down to 130 nm.
b) Predict the performance potential of decanano SiGe devices in the ballistic transport regime, correctly accounting for interface issues, atomistic and other fluctuation effects, and realistic device parasitics.
c) Develop design strategies to optimise performance and provide a measure of immunity to fluctuation effects.

Project Achievements to date:

The project began in March 2001.

- Coupled n- and p- channel 2D full band Monte Carlo, finite element simulator for complete CMOS simulation with extensive RF analysis capability.
- New theory of quantum corrections due to variable effective mass arising from graded SiGe structures.

• New studies of the incorporation of quantum effects via the quantum potential model
• Increased understanding of how to simulate device performance in deep sub-micron silicon-germanium technology.
• New multigrid algorithm for rapid simulation
• New fast algorithm for calculating interface roughnesss scattering from direct quantum simulations.

The previous phase of the project (Phase I) was assessed recently by EPSRC and achieved an overall assessment of Outstanding. Phase I yielded 16 journal and conference publications from the device modelling group.

Outline of current work
The Device Modelling Group at Glasgow University is part of the large EPSERC multi-university grant entitled 'SiGe for MOS Technologies', which is now in Phase II. Device Modelling is a core activity within this consortium activity, and provides the following services and resources:

- The rapid provision, analysis and optimisation of the basic designs for SiGe and strained Si layered structures and the fabrication of devices.
- The development of a hierarchy of simulation tools ranging from *ab initio* methodologies through to circuit simulation models, incorporating new physical models where appropriate and tailoring them for SiGe systems.
- The provision of lead time and look-ahead for the experimental programme by using the predictive power of modelling to evaluate the best experimental design routes.
- Provision of training to members of the consortium in the use of the modified commercial simulation tools for day-to-day work.

As part of this grant we have developed, for the first time in the UK, a world class Full Band (FB) Monte Carlo simulator for investigation of hole transport properties both in bulk [i] and in real (finite geometry) SiGe devices [ii] (Figure 1.). Improved interface roughness scattering [iii] and alloy scattering models have and are continued to be developed, calibrated and validated against experimental data.

The FB model is essential for describing hole transport in strained and unstrained material, because of the complex warped constant energy surfaces. It is based on a 6-band (3 + spin) **k·p** calculation, discretised around the whole Brillioun zone (Figure 2.). Important transport effects [iv,v] derived from the complex hole band structure have been explored and enhancement of device performance due to transient effects have been predicted [vi,vii,viii]. The bulk code has been used to obtain transport parameters, including mobility, saturation velocity, energy dependent energy and momentum relaxation times, which are essential input parameters for commercial simulators. Within the grant we have also begun to investigate a variety of methods for including to first order quantum effects, such as size quantization and tunnelling, into semi-classical device models, both Drift Diffusion [ix,x] and Monte Carlo [xi] based on moments and expansions of the Wigner equation of motion.

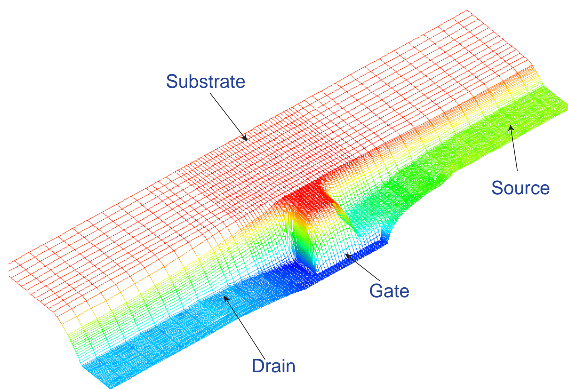

Figure 1: Potential profile across a deep sub-micron *p*-MOSFET, obtain from our Full-Band, finite element device simulator.

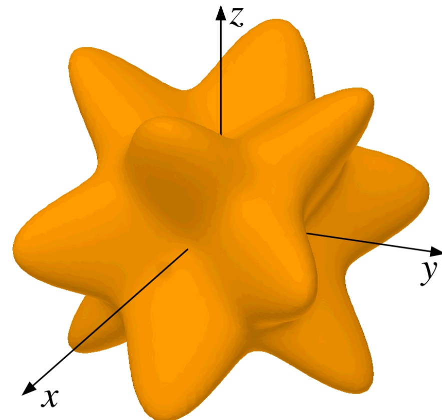

Figure 2: Anisotropic isoenergy surface at ~40 meV (T=300K), for the heavy hole |3/2,3/2> band in Si calculated from **k•p**.

A 3D Monte Carlo simulator is also being developed which incorpates *ab initio* Coulomb scattering for both donors and carriers [xii], coupling this to our bandstructure models will provides us with some of the tools, that are likely to be crucial for modelling *aggressively scaled* device architecture where non-equilibrium transport, hot carrier effects, atomistic affects and geometrical effects become important.

We have also developed a variety of new numerical techniques, such as a multigrid technique [xiii], allowing extremely rapid solution of the non-linear partial differential equations, which are common within device modelling.

Additionally we have developed a new algorithm, which allows us to solve fast, and accurately the time-dependent multi-dimensional (2 and 3-D) Schrödinger equation, which has been used to study *ab inito* interface roughness scattering [iii] (Figure 4.). Therefore many of the techniques we have and are continuing to develop under the SiGe grant will provide us with some of the tools and skills that will be required for the work we propose to carry out under the Platform Grant.

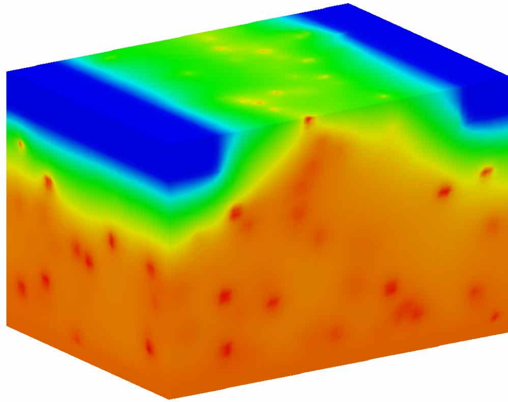

Figure 3: Potential profile obtained from our 3-D Full Band *p*-MOSFET, including *ab-inito* Coulomic scattering. Solution was obtained using our multigrid algorithm.

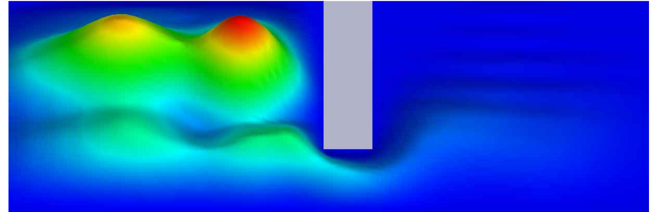

Figure 4: Wave packet simulation snap-shot of a quantum wave-packet scattering through a throttle region, into an open quantum dot, obtained from our 2-D time-dependent Schrödinger equation.

Publications:

i J. R. Watling, A. Asenov and J. R. Barker, "Efficient Hole Transport Models in Warped Bands for use in the simulations of Si/SiGe MOSFETs", IWCE-6 (Osaka). IEEE No. 98EX116

ii J. R. Watling, Y. P. Zhao, A. Asenov and J. R. Barker, "Non-equilibrium hole transport in deep sub-micron Well-Tempered Si p-MOSFETs", to be published in VLSI Design (2001).

iii J. R. Barker, J. R. Watling and R. C. W. Wilkins "A fast algorithm for the study of wave-packet scattering at disordered interfaces", to be published in VLSI Design (2001).

iv J. R. Barker, "Warped Valence Bands in Si/SiGe and their influence on device performance", invited talk, CMMP-99.

v J. R. Barker and J. R. Watling, "Simulation of enhanced interface trapping due to carrier dynamics in warped valence bands in SiGe devices", to be published in VLSI Design (2001).

vi S. Kaya, Y. P. Zhao, J. R. Watling, A. Asenov, J. R. Barker, G. Ansaripour, G. Braithwaite, T. E. Whall and E. H. C. Parker "Indication of velocity overshoot in strained $Si_{0.8}Ge_{.2}$ *p*-channel MOSFETs" Semiconductor Science and Technology 15 p573-578 (2000).

vii Y. P. Zhao, S.Kaya, J. R. Watling, A. Asenov, J. R. Barker, M. Palmer, G. Braithwaite, T. E. Whall, E. H. C. Parker, A. Waite and A. G. R. Evans "Indication of non-equilibrium transport in SiGe *p*-MOSFETs" proceedings of ESSDERC 2000 p224-227.

viii Y. P. Zhao, J. R. Watling, S. Kaya, A. Asenov and J. R. Barker "Drift Diffusion and hydrodynamic simulations of Si/SiGe *p*-MOSFETs" Materials Science and Engineering B-Solid State Materials for Advanced Technology 72 p180-183 (2000)

ix J. R. Watling, A. R. Brown, A. Asenov and D. K. Ferry, "Quantum Corrections in 3-D Drift Diffusion Simulations of Decanano MOSFETs Using and Effective Potential", published in the proceedings of SISPAD' 2001.

x J. R. Watling, A. R. Brown and A. Asenov, "Can the density gradient approach describe the source-drain tunnelling in decanano double-gate MOSFETs ?", to be published in the Journal of Computational Electronics, 2002.

xi J. R. Watling, J. R. Barker and S. Roy, "Quantum Potential Corrections for Spatially Dependent Effective Masses with Application to Charge Confinement at Heterostructure Interfaces", to be published in the Journal of Computational Electronics, 2002.

xii J. R. Watling, J. R. Barker and A. Asenov "Soft sphere model for electron correlation and scattering in the atomistic modelling of semiconductor devices" to be published in VLSI Design (2001).